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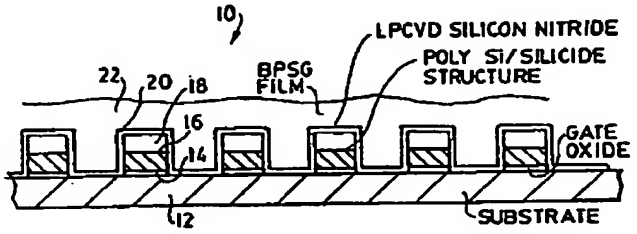
(54) Method of forming a doped silicon oxide film

(57) A process is provided for the low temperature deposition of a thin film of borophosphosilicate glass (BPSG) for use in semiconductor devices, such as DRAMs. The process includes utilizing R-OH groups as reagents to provide additional -OH groups so that an intermediate $[Si(OH)_4]_n$ is formed having superior reflow properties, allowing the annealing and reflow steps to occur at temperatures less than 750°C, which is the current processing temperature.



TYPICAL GATE CONDUCTOR STRUCTURE TO BE FILLED WITH BPSG FILM.

FIG.1

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Description

This invention generally relates to a method for fabricating semiconductors, and more particularly, a method for providing a doped silicon oxide film on a semiconductor substrate.

In recent years, progress in the miniaturization and multilayer interconnection of semiconductor devices has led to an increase in the aspect ratio, with the result that uneven portions on the surface of a pattern have a serious influence on the reliability of the device. For this reason, the development of a process or material for the formation of a semiconductor device which enables better planarizing of an interlayer insulation film provided between wiring layers has been a driving force behind much research.

Borophosphosilicate glass ("BPSG") films or layers exhibit good planarizing properties and are therefore especially important in highly dense dynamic random access memories ("DRAMs"), especially in advanced DRAMs having increased stacked capacitor heights and ultra high integration densities. Typically, however, BPSG reflow or annealing requires high temperature processes, which cause device breakdown because of thermal stress and unwanted dopant diffusion. Additionally, the high temperatures may be detrimental to the advanced silicides currently used for ultra large scale integrated circuits ("ULSI"), such as cobalt silicide, titanium silicide, and nickel silicide.

In order to deal with these problems, related art methods of improving the deposition temperature have included increasing the annealing time and doping the films with germanium (Ge) to reduce the processing temperature to approximately 700°C. However, Ge doping requires a longer process time, therefore decreasing production, and results in lower film quality, which in turn renders it incompatible with current ULSI processing.

It has been shown in more recent studies that the reflow properties of oxide films can be enhanced by reacting silane with peroxide at a temperature in the range of 0-50°C as follows:

$$SiH_4 + H_2O_2 \Rightarrow Si(OH)_4$$

The reflowed polymerized siloxane formed yields good gap filling of the interlevel metals. However, the as-deposited film is of poor quality and must be made more dense by high temperature annealing. Furthermore, the processing time is generally long when compared to other processes. This process can only be implemented at low temperatures (0-50°C) because H_2O_2 decomposes rapidly at higher temperatures. As a result, the deposition can only be implemented in multi-step processes and with lower quality films. Additionally, the process has only been developed for undoped oxides. However, boron and/or phosphorus doped oxides are required in many applications for mobile ion gettering and to allow high etch rates during contact hole etching. Incorporation of higher concentrations (>5 wt%) of boron and phosphorus dopants may increase crystal defect formation on the deposited film. This will subsequently have a detrimental effect on ULSI and VLSI device fabrication.

Accordingly the present invention provides a process for forming a thin film of a doped silicon oxide on a semiconductor structure comprising the steps of:

depositing a thin film of the doped silicon oxide onto the semiconductor structure at a temperature of less than 750°C;
annealing the thin film of the silicon oxide *in situ*; and
depositing a final thin film of the silicon oxide onto the thin film at a temperature of less than 750°C.

In the preferred embodiment, the process further comprises the step of providing a silicon source; a boron source; a phosphorus source; an oxygen source; and a hydroxide source. Preferably the silicon source is selected from the group consisting of: silane and TEOS; the boron source is selected from the group consisting of: diborane, trimethyl borate, and triethyl borate; the phosphorus source is selected from the group consisting of: phosphene, trimethyl phosphate, and triethyl phosphate; the oxygen source is selected from the group consisting of: oxygen, nitrous oxide, and ozone; and the hydroxide source is selected from the group consisting of: R-OH, wherein R is H, an alkyl group, a benzyl group, or a double bond carbon.

The invention also provides a borophosphosilicate glass (BPSG) film formed by such a process, and an integrated circuit chip including a semiconductor structure and such a BPSG film.

Thus hydroxyl groups may be introduced to the BPSG chemical vapor deposition (CVD) system to achieve low temperature reflow, both during deposition and during the subsequent annealing steps, with the BPSG film being formed by depositing a thin BPSG film onto a surface; in situ annealing of the film; and depositing a final thin layer of BPSG film.

This approach provides good gap fill and high planarization capability, and also the ability to getter mobile ions such as potassium and sodium is maintained without additional processing steps. Importantly, the processing temperature of the BPSG films is reduced below current process temperatures of 750 - 850°C, therefore rendering the process suitable for the advanced silicides used in ULSI. This process utilizes the advantages of hydroxyl groups that are more stable than H_2O_2 to enable processing at higher temperatures (>50°C) but still low enough temperatures (<700°C) for

advanced silicide applications. Furthermore, unwanted dopant diffusion and thermal stress are reduced by the lower temperature processing.

It is preferable to also reduce the amount of steps and/or time it takes to process the silicide film so that throughput rates are optimized. By utilizing a simple, three step process, the process described herein reduces the time necessary to process the silicide layer while filling the sub-0.25μm gaps and voiding while still partially planarizing the surface.

A preferred embodiment of the invention will now be described by way of example only, with reference to the following drawings:

FIG. 1 is a diagrammatic cross-sectional view of a gate structure in accordance with the present invention;
and FIGS. 2A and 2B are SEMs of the typical gate conductor structure in accordance with the present invention.

A thin film of BPSG is deposited onto a surface that includes gate conductor structures of sub-half micron topography as shown in FIG. 1. The structure 10 includes a gate oxide layer 12, a polysilicone/silicate layer 14, a silicon nitride layer and a thin film layer 20. The BPSG layer 22 is deposited on the surface of all of these layers. The final structure is shown in the scanning electron micrographs as shown in FIGS. 2A and 2B.

The reactants used to form the BPSG film are: silicon; oxygen; phosphorus; boron and R-OH, wherein R is selected from the group consisting of: H and any organic groups, such as alkyl, double bond carbons, or benzyl groups. This group can be varied to increase or decrease the stability of the -OH groups depending on process conditions. Further, carbon chains of 1-10 carbons in length are preferred, however, longer chains may be used provided process parameters are manipulated to allow these carbon chains to be added to the silicone oxide.

The silicon is typically provided as tetraethylorthosilicate ("TEOS"), silane (SiH_4), or a mixture of the two. The phosphorus is provided as phosphine (PH_3), although alternative sources such as trimethyl phosphate ("TMP") or triethyl phosphate ("TEP") may also be used to reduce toxicity and reactivity. Oxygen is provided in the form of oxygen gas in its normal (O_2) state, although nitrous oxide or ozone may also be used. The boron is preferably provided as triethyl borate ("TEP"), however, diborane and trimethyl borate ("TMB") may also be used. Additionally, R-OH compounds are used to enhance the reflow and reduce the temperature at which the deposition and reflow or annealing steps take place. Thus, the deposition reactions are as follows:

$$TEOS + PH_3 + TEB + R\text{-}OH \xrightarrow{<750°C} BPSG\ film$$

$$SiH_4 + PH_3 + TEB + R\text{-}OH \xrightarrow{<750°C} BPSG\ film$$

$$SiH_4 + TEOS + PH_3 + TEB + R\text{-}OH \xrightarrow{<750°C} BPSG\ film$$

wherein R is H, CH_3, C_2H_5, C_6H_5, or any other alkyl or double bond carbon organic compound.

It should be noted that, because the deposition of the BPSG film is conducted at a relatively high temperature (>500°C), most R-OH species will be dissociated into the R group and the hydroxide group. Thus, the introduction of the R-OH groups to the reaction mixture generates more -OH groups during the deposition annealing and final planarization deposition. The hydroxide groups will then react with the silicon in either the silane or the TEOS and form mobile $\{Si(OH)_4\}_n$ groups, which in turn enhance the reflow properties of the film. As a result, the gap-filling properties of the process at lower processing temperatures are observed to be as good as current processing methods (without the hydroxyl groups) at higher temperatures are observed.

FIGS. 2A and 2B illustrate examples of the gap filling produced for gate conductors in accordance with the process of the present invention.

To recap therefore, the low pressure, relatively low temperature, chemical vapor deposition process disclosed herein allows filling of the sub-0.25 μm voids and partial planarization of the surface. After deposition of a thin film of BPSG, an *in situ* anneal step is typically performed at 600-700°C for 1-60 min., followed by deposition of a final thin film of BPSG. Low temperature reflow of borophosphosilicate glass (BPSG) is achieved both during deposition and subsequent annealing. This process may be conducted for example in an Integrity tool by LAM, Inc. of Freemont, CA.

Claims

1. A process for forming a thin film of a doped silicon oxide on a semiconductor structure comprising the steps of:

depositing a thin film of the doped silicon oxide onto the semiconductor structure at a temperature of less than 750°C;
annealing the thin film of the silicon oxide *in situ*; and
depositing a final thin film of the silicon oxide onto the thin film at a temperature of less than 750°C.

2. The process of claim 1, further comprising the step of providing a silicon source; a boron source; a phosphorus source; an oxygen source; and a hydroxide source.

3. The process of claim 2, wherein the silicon source is selected from the group consisting of: silane and TEOS.

4. The process of claim 2 or 3, wherein the boron source is selected from the group consisting of: diborane; trimethyl borate; and triethyl borate.

5. The process of claim 2, 3, or 4, wherein the phosphorus source is selected from the group consisting of: phosphene; trimethyl phosphate; and triethyl phosphate.

6. The process of claim 2, 3, 4, or 5, wherein the oxygen source is selected from the group consisting of: oxygen; nitrous oxide; and ozone.

7. The process of claim 2, 3, 4, 5, or 6, wherein the hydroxide source is selected from the group consisting of: R-OH, wherein R is H; an alkyl group; a benzyl group; or a double bond carbon.

8. A borophosphosilicate glass (BPSG) film formed by the process of any preceding claim.

9. An integrated circuit chip including a semiconductor structure and the BPSG film of claim 8.

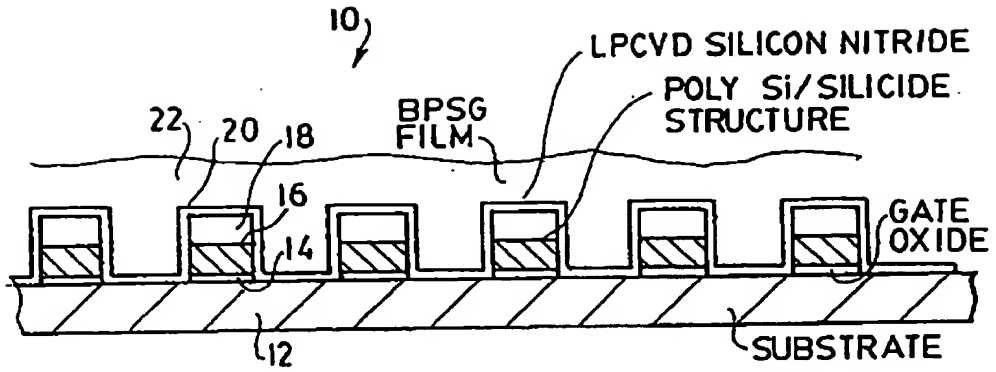

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FIG.1

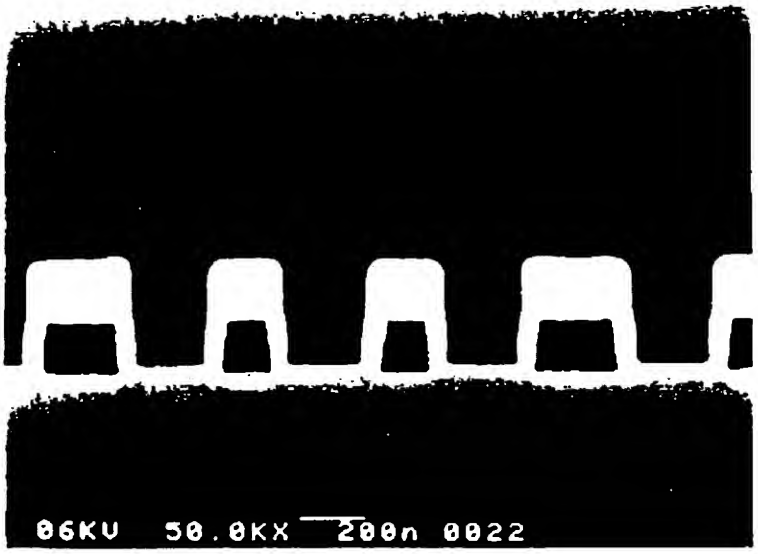

FIG. 2A

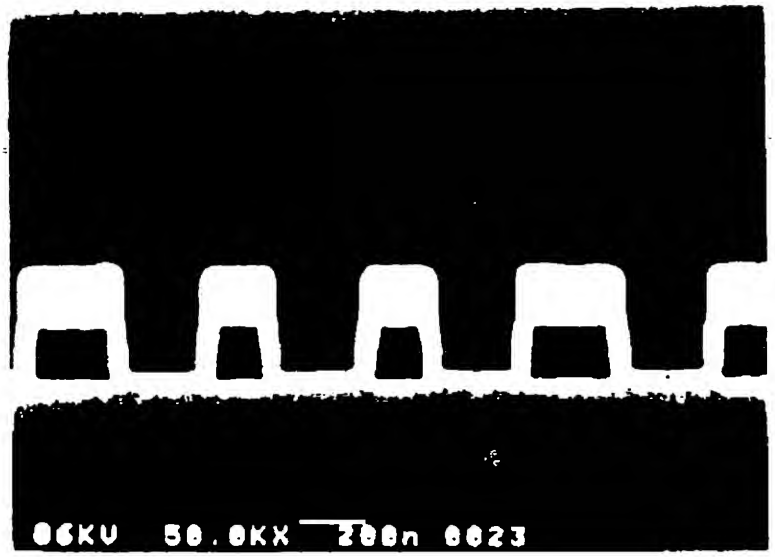

FIG. 2B

A TYPICAL GATE CONDUCTOR STRUCTURE SUB-HALF MICRON FILLED WITH BPSG FILM AT <750°C.

FIG. 2

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 30 4053

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	EP 0 677 869 A (SGS THOMSON MICROELECTRONICS) 18 October 1995 * column 3, line 47 - column 5, line 28; claims 1-4 *	1-7	H01L21/3105 H01L21/316
A	US 4 835 597 A (OKUYAMA YASUSHI ET AL) 30 May 1989 * column 4, line 2-15 *	1-7	
A	US 5 094 984 A (LIU CHARLES C ET AL) 10 March 1992 * column 3, line 43 - column 7, line 37 *	1-7	
A	PATENT ABSTRACTS OF JAPAN vol. 018, no. 035 (E-1494), 19 January 1994 & JP 05 267480 A (RICOH CO LTD), 15 October 1993, * abstract *	1-5	
A	PATENT ABSTRACTS OF JAPAN vol. 015, no. 058 (E-1032), 12 February 1991 & JP 02 284425 A (NEC CORP), 21 November 1990, * abstract *	1	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L
A	DOBSON C D ET AL: "ADVANCED SIO2 PLANARIZATION USING SILANE AND H2O2" SEMICONDUCTOR INTERNATIONAL, vol. 17, no. 14, page 85/86, 88 XP000671223 * the whole document *		

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	14 October 1997	Boetticher, H

CATEGORY OF CITED DOCUMENTS

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